AMENDMENTS TO THE CLAIMS

1-30. (Canceled)

31. (Currently Amended) A system comprising:

~~an active~~a first host system executing a first plurality of applications via a first plurality of buses; and

a ~~standby~~ second host system executing a second plurality of applications via a second plurality of buses, and the second host system coupled with the ~~active~~ first host system via a ~~plurality of buses~~communications link, wherein the ~~active~~ first host system and the ~~standby~~ second host system each include a controller, the controller having

a fault detection module coupled with fault detection hardware, the fault detection module to receive a notification from the fault detection hardware indicating a fault of either the first host system or the second host system, wherein when the fault occurs, the plurality of applications corresponding to the host system that failed are executed via the plurality of buses of the host system that is still active,

~~a bus arbiter control module to provide bus arbitration on the plurality of buses, and to coordinate control of the plurality of buses between the active host and the standby host,~~ and

a host control (HC) interface unit to generate control signals transmitted during startup and fail-over.

32. (Currently Amended) The system of claim 31, wherein the controller further comprises:

an interface to provide the controller with access to ~~programs running~~ the first and second plurality of applications being executed on the ~~active~~first host system and the ~~standby~~second host system;

a Peripheral Component Interconnect (PCI)-to-PCI (P2P) control module;

a power and reset control module; and

a clock control module to provide clock signals to the first and second plurality of buses.

33. (Currently Amended) The system of claim 31, wherein the first and second plurality of buses ~~comprises~~ comprise a first and second plurality of COMPACTPCI buses.

34. (Previously Presented) The system of claim 31 to use a Redundant System Slot (RSS) architecture.

35. (Currently Amended) The system of claim 32, wherein the ~~active~~first host system and the ~~standby~~second host system each include a plurality communication modules, and an Ethernet link coupled with the plurality of communication modules to maintain synchronization between the ~~active~~first host system and the ~~standby~~second host system.

36. (Previously Presented) The system of claim 31, wherein the HC interface unit is further to:

receive control signals transmitted during startup and fail-over; and

respond to control signals transmitted during startup and fail-over.

37. (Currently Amended) A method comprising:

executing a first plurality of applications on a first host system via a first plurality of buses;

executing a second plurality of applications on a second host system via a second plurality of buses;

receiving a notification from fault hardware indicating a fault of either the first host system or the second host system, wherein when the fault occurs, the plurality of applications corresponding to the host system that failed are executed via the plurality of buses of the host system that is still active;

~~providing bus arbitration on a plurality of buses;~~

~~coordinating control of the plurality of buses between an active host and a standby host~~; and

generating control signals to be transmitted during startup and fail-over.

38. (Currently Amended) The method of claim 37, further comprising:

accessing ~~programs running~~the first and second plurality of applications being executed on the ~~active~~first host system and the ~~standby~~second host system; and

providing clock signals to the plurality of buses.

39. (Currently Amended) The method of claim 37, wherein the first and second plurality of buses ~~comprises~~ comprise a first and second plurality of COMPACTPCI buses.

40. (Currently Amended) The method of claim 38, further comprising maintaining synchronization between the ~~active~~first host system and the ~~standby~~second host system via an Ethernet link.

41. (Previously Presented) The method of claim 37, further comprising:
receiving the control signals to be used during startup and fail-over; and
responding to the control signals received during startup and fail-over.

42-44. (Canceled)

45. (Currently Amended) A controller comprising:
a fault detection module coupled with fault detection hardware, the fault detection module to receive a notification from the fault detection hardware indicating a fault of either a first host system or a second host system, wherein when the fault occurs, a plurality of applications corresponding to the host system that failed are executed via a plurality of buses of the host system that is still active;
~~a bus arbiter control module to provide bus arbitration on a plurality of buses, and to coordinate control of the plurality of buses between an active host and a standby host~~; and

a host control (HC) interface unit to generate control signals transmitted during startup and fail-over.

46. (Currently Amended) The controller of claim 45, wherein the controller further comprises:

an interface to provide the controller with access to ~~programs running~~the plurality of applications being executed on the ~~active~~first host system and the ~~standby~~second host system;

a Peripheral Component Interconnect (PCI)-to-PCI (P2P) control module;

a power and reset control module; and

a clock control module to provide clock signals to the plurality of buses.

47. (Currently Amended) The controller of claim 45, wherein the first and second plurality of buses ~~comprises~~ comprise a first and second plurality of COMPACTPCI buses.

48. (Previously Presented) The controller of claim 45 to use a Redundant System Slot (RSS) architecture.

49. (Currently Amended) The ~~system~~ controller of claim 45, wherein the HC interface unit is further to:

receive control signals transmitted during startup and fail-over; and

respond to control signals transmitted during startup and fail-over.